REMARKS

These remarks follow the order of the paragraphs of the office action. Relevant portions of the office action are shown indented and italicized.

Application/Control Number: 10/61 9,989   *Page 2*
Art Unit: 2182

DETAILED ACTION

Claim Rejections - 35 USC ~ 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 1-10, 17-18, 21-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites a "buffer storing indications of events" in line 2,

In response, the applicants respectfully states that...

The phrase buffer storing indications of events is stated on page 2, line 4.

The office communication continues:

"said apparatus for transferring interrupts from the peripheral device to a host computer"

1   In response, the applicants respectfully states that the phrase said apparatus for transferring

2   interrupts from the peripheral device to a host computer is stated on page 44, line 5.

3   The office communication continues:

4   *in lines 3-4", moving the contents of the buffer to the payload portion of the control data*
5   *block, and sending the control data block to the host computer system"*

6   In response, the applicants respectfully states that the phrase moving the contents of the buffer to

7   the payload portion of the control data block, and sending the control data block to the host

8   computer system is stated on page 2, line 6.

9   The office communication continues:

10   *in lines 7-9. The recitations suggest that indications of events are stored in the buffer and*
11   *that the indications of events (the contents of the buffer) are moved to a payload portion*
12   *of the control data block and sending the control data block to the host computer system.*
13   *The recitations also suggest that only interrupts from the indications of events (i.e. not*
14   *the indications of events) are transferred from the peripheral device to the host computer*
15   *system. It appears that the specification only discloses transferring all indications of*
16   *events in the control block to the host computer.*

17   *3. Claims 11-16, 19-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply*

18   *with the enablement requirement. The claim(s) contains subject matter, which was not described*

19   *in the specification in such a way as to enable one skilled in the art to which it pertains, or with*

20   *which it is most nearly connected, to make and/or use the invention.*

21   *It appears that there is no support for "moving the contents of the buffer to the corresponding*

22   *fields of the payload portion"*

23   In response, the applicants respectfully states that moving the contents of the buffer to the
24   corresponding fields of the payload portion is stated on page 44, line 10

25   The office communication continues:

1   *- as page 38, lines 25-26 merely discloses "when preset conditions are met, an Interrupt*
2   *Control Block (ICB) 1680 is generated by the ISOC 120 from the information stored in*
3   *the interrupt FIFO 1660".*

4   *4.   Claims 13-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply*
5   *with the enablement requirement. The claim(s) contains subject matter, which was not*
6   *described in the specification in such a way as to enable one skilled in the art to which it*
7   *pertains, or with which it is most nearly connected, to make and/or use the invention.*

8   In response, the applicants respectfully states that...

9   *Claim 13 recites "at least a predetermined plurality of indications is stored in the*
10   *buffer".*
11   In response, the applicants respectfully states that the phrase at least a predetermined
12   plurality of indications is stored in the buffer is stated on page 5, line 2

13   The office communication continues:

14   *Claim 14 recites "at least one indication is stored in the buffer".*

15   In response, the applicants respectfully state that the phrase at least one indication is stored in the
16   buffer is stated on page 5, line 4

17   The office communication continues:

18   *Claim 15 recites "a count indicative of the number of indications included in the payload*
19   *portion".*
20   In response, the applicants respectfully state the phrase a count indicative of the number of
21   indications included in the payload portion is stated on page 5, line 7

22   The office communication continues:

23   *Claim 1 suggests storing only interrupts in the buffer and does not suggest storing*
24   *indications other than interrupts in the buffer. The claims suggest that interrupts and*
25   *indications are two different entities, while the specification only discloses only one entity*
26   *being stored in the buffer and the count being indicative of only one entity.*

27   *5. Claims 10, 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the*

28   *enablement requirement. The claim(s) contains subject matter, which was not described in the*

29   *specification in such a way as to enable one skilled in the art to which it pertains, or with which*

30   *it is most nearly connected, to make and/or use the invention. The examiner cannot find support*

31   *for the limitations of the claims. In particular, it is not clear what constitute the claimed*

32   *apparatus, the claimed host processing system, the claimed memory of the host processing*

1   *system, the claimed data processing system, the claimed host computer, and the claimed memory*

2   *of the host computer system. Applicant is required to specifically point out where to find the*

3   *support for the limitations of the claims in the specification, by page and line number -and in*

4   *particular, applicant is required to map out each of the elements claimed with the teachings of*

5   *the specification.*

6   *6.   No art rejection was made to claims 1-16, 21-22 because the scope of the claims is*

7   *ambiguous, and it is not possible for the examiner to apply prior art without making a great deal*

8   *of speculation.*

9   ***Claim Rejections -35 USC § 102***

10 *7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form*
11 *the basis for the rejections under this section made in this Office action:*

12 *A person shall be entitled to a patent unless —*

13 *(b) the invention was patented or described in a printed publication in this or a foreign*
14 *country or in public use or on sale in this country, more than one year prior to the date*
15 *of application for patent in the United States.*

16 *8.   Claims 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated Raasch et al.*
17 *(US 5,333,273).*
18 In response, the applicant respectfully states that Claims 17-20 are made patentable by the

19 invention of Raasch. The present invention, claimed in Claims 17-20, provides: (see pto abstract)

20 Whereas, the cited art to Raasch, US Patent 5,333,273, filed: September 3, 1992 is entitled:

21 "Protected hot key function for microprocessor-based computer system". The abstract reads: "An

22 ISA-compatible computer system includes an additional function key on its keyboard. The

23 additional function key does not have a defined function for conventional ISA-standard

24 computers. When a conventional alphanumeric key or function key is activated on the keyboard,

25 the computer system is interrupted using IRQ1 and the key information is communicated to the

26 computer system so that the computer system can respond in a conventional manner using a

27 conventional keyboard interrupt handling routine. When the additional function key and an

1   alphanumeric key are activated in combination, a second interrupt different from the IRQ1

2   interrupt is activated (e.g., IRQ15). The computer system responds to the second interrupt by

3   inputting an identification of the activated alphanumeric key and performing a selected

4   predetermined function in response thereto. The handling of the second interrupt is performed by

5   a separate interrupt handling routine within the computer system so that conventional terminate

6   and stay resident (TSR) programs that intercept conventional keyboard inputs cannot readily

7   intercept keyboard input initiated by the additional function key".

8   *9.   As per claims 17, 19, Raasch teaches a computer program product (or article of*
9   *manufacture) comprising a computer usable medium [138, FIG. 1] having computer*
10   *readable program code means [BIOS: col. 5, lines 18-21] embodied therein for causing*
11   *transfer of interrupts [col. 4, lines 66-68], the computer readable program code means in*
12   *said computer program product (or article of manufacture) comprising computer*
13   *readable program code means [BIOS: col. 5, lines 18-21] for causing a computer [100,*
14   *FIG. 1] to effect the functions of the apparatus of claim 1 (or the method of claim 11) -as*
15   *the BIOS would cause a computer to effect the functions of any apparatus, hence*
16   *including functions of the apparatus of claim 1; and as the BIOS would cause a computer*
17   *to effect the steps of any method, hence including the steps of the method of claim 11.*
18   *Application/Control Number: 10/61 9,989   Page 2*
19   *Art Unit: 2182*

20   ***DETAILED ACTION***

21   ***Continued Examination Under 37 CFR 1.114***

22   *1. A request for continued examination under 37 CFR 1.114, including the fee set forth in*
23   *37 CFR 1.17(e), was filed in this application after final rejection. Since this application*
24   *is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37*
25   *CFR 1.17(e) has been timely paid, the finality of the previous Office action has been*
26   *withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 29, 2007 has*
27   *been entered.*

28   ***Claim Rejections - 35 USC ~ 112***

29   *1. The following is a quotation of the first paragraph of 35 U.S.C. 112:*

30   *The specification shall contain a written description of the invention, and of the manner*
31   *and process of making and using it, in such full, clear, concise, and exact terms as to*
32   *enable any person skilled in the art to which it pertains, or with which it is most nearly*
33   *connected, to make and use the same and shall set forth the best mode contemplated by*
34   *the inventor of carrying out his invention.*

1   *The following is a quotation of the second paragraph of 35 U.S.C. 112:*

2   *The specification shall conclude with one or more claims particularly pointing out and*
3   *distinctly claiming the subject matter, which the applicant regards as his invention.*

4   *2. Claims 1-10, 17-18, 21-22 are rejected under 35 U.S.C. 112, first paragraph, as failing*
5   *to comply with the enablement requirement. The claim(s) contains subject matter, which*
6   *was not described in the specification in such a way as to enable one skilled in the art to*
7   *which it pertains, or with which it is most nearly connected, to make and/or use the*
8   *invention.*

9   *Claim 1 recites a "buffer storing indications of events" in line 2, "said apparatus for*
10   *transferring interrupts from the peripheral device to a host computer" in lines 3-4",*
11   *moving the contents of the buffer to the payload portion of the control data block, and*
12   *sending the control data block to the host computer system" in lines 7-9. The recitations*
13   *suggest that indications of events are stored in the buffer and that the indications of*
14   *events (the contents of the buffer) are moved to a payload portion of the control data*
15   *block and sending the control data block to the host computer system. The recitations*
16   *also suggest that only interrupts from the indications of events (i.e. not the indications of*
17   *events) are transferred from the peripheral device to the host computer system. It appears*
18   *that the specification only discloses transferring all indications of events in the control*
19   *block to the host computer.*

20   *3. Claims 11-16, 19-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply*

21   *with the enablement requirement. The claim(s) contains subject matter, which was not described*

22   *in the specification in such a way as to enable one skilled in the art to which it pertains, or with*

23   *which it is most nearly connected, to make and/or use the invention.*

24   *It appears that there is no support for "moving the contents of the buffer to the corresponding*

25   *fields of the payload portion" - as page 38, lines 25-26 merely discloses "when preset conditions*

26   *are met, an Interrupt Control Block (ICB) 1680 is generated by the ISOC 120 from the*

27   *information stored in the interrupt FIFO 1660".*

28   *4. Claims 13-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the*

29   *enablement requirement. The claim(s) contains subject matter, which was not described in the*

30   *specification in such a way as to enable one skilled in the art to which it pertains, or with which*

31   *it is most nearly connected, to make and/or use the invention.*

1 *Claim 13 recites "at least a predetermined plurality of indications is stored in the buffer". Claim*
2 *14 recites "at least one indication is stored in the buffer". Claim 15 recites "a count indicative*
3 *of the number of indications included in the payload portion". Claim 1 suggests storing only*
4 *interrupts in the buffer and does not suggest storing indications other than interrupts in the*
5 *buffer. The claims suggest that interrupts and indications are two different entities, while the*
6 *specification only discloses only one entity being stored in the buffer and the count being*
7 *indicative of only one entity.*

8 *5. Claims 10, 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the*
9 *enablement requirement. The claim(s) contains subject matter, which was not described in the*
10 *specification in such a way as to enable one skilled in the art to which it pertains, or with which*
11 *it is most nearly connected, to make and/or use the invention. The examiner cannot find support*
12 *for the limitations of the claims. In particular, it is not clear what constitute <u>the claimed</u>*
13 *<u>apparatus</u>, <u>the claimed host processing system</u>, <u>the claimed memory of</u> <u>the host processing</u>*
14 *<u>system</u>, <u>the claimed data processing system</u>, <u>the claimed host computer</u>, and <u>the claimed memory</u>*
15 *<u>of the host computer system</u>. Applicant is required to specifically point out where to find the*
16 *support for the limitations of the claims in the specification, by page and line number -and in*
17 *particular, applicant is required to map out each of the elements claimed with the teachings of*
18 *the specification.*

19 *6. No art rejection was made to claims 1-16, 21-22 because the scope of the claims is*
20 *ambiguous, and it is not possible for the examiner to apply prior art without making a*
21 *great deal of speculation.*

22 In response, the applicants respectfully states that it is believed that the support provided would
23 provide what is apparently not understood previously. Thus claims 1-16 are allowable.

24 ### *Claim Rejections -35 USC § 102*
25 *7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that*
26 *form the basis for the rejections under this section made in this Office action: A person*
27 *shall be entitled to a patent unless -*

1 *(b) the invention was patented or described in a printers publication in this or a foreign*
2 *country or in public use or on sale in this country, more than one year prior to the date*
3 *of application for patent in the United States.*

4   *8. Claims 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated Raasch et al.*
5 *(US 5,333,273).*

6 In response, the applicant respectfully states that Claims 17-20 are not made patentable by the

7 invention of Raasch. The present invention, claimed in Claims 17-20, provides:

8   "Methods, systems and apparatus for transferring interrupts from a peripheral device to a

9   host computer system is described. In an example embodiment, an apparatus comprises a

10   buffer for storing indications of interrupts generated by the peripheral device. In response

11   to a preset condition being met, a controller generates a control data block having a

12   payload portion, moves the contents of the buffer to the payload portion of the control

13   data block, and sends the control data block to the host computer system."

14 Whereas, the cited art to Raasch, US Patent 5,333,273, filed: September 3, 1992, is entitled:

15 "Protected hot key function for microprocessor-based computer system". The abstract reads: "An

16 ISA-compatible computer system includes an additional function key on its keyboard. The

17 additional function key does not have a defined function for conventional ISA-standard

18 computers. When a conventional alphanumeric key or function key is activated on the keyboard,

19 the computer system is interrupted using IRQ1 and the key information is communicated to the

20 computer system so that the computer system can respond in a conventional manner using a

21 conventional keyboard interrupt handling routine. When the additional function key and an

22 alphanumeric key are activated in combination, a second interrupt different from the IRQ1

23 interrupt is activated (e.g., IRQ15). The computer system responds to the second interrupt by

24 inputting an identification of the activated alphanumeric key and performing a selected

25 predetermined function in response thereto. The handling of the second interrupt is performed by

26 a separate interrupt handling routine within the computer system so that conventional terminate

27 and stay resident (TSR) programs that intercept conventional keyboard inputs cannot readily

28 intercept keyboard input initiated by the additional function key ". Thus Raasch is not concerned

1 with or teach. indications of events or a preset condition as in the claims. Thus, all claims are

2 allowable.

3   *9. As per claims 17, 19, Raasch teaches a computer program product (or article of*
4 *manufacture) comprising a computer usable medium [138, FIG. 1] having computer*
5 *readable program code means [BIOS: col. 5, lines 18-21] embodied therein for causing*
6 *transfer of interrupts [col. 4, lines 66-68], the computer readable program code means in*
7 *said computer program product (or article of manufacture) comprising computer*
8 *readable program code means [BIOS: col. 5, lines 18-21] for causing a computer (100,*
9 *FIG. 1] to effect the functions of the apparatus of claim 1 (or the method of claim 11)- as*
10 *the BIOS would cause a computer to effect the functions of any apparatus, hence*
11 *including functions of the apparatus of claim 1; and as the BIOS would cause a computer*
12 *to effect the steps of any method, hence including the steps of the method of claim 11.*

13   *10. As per claim 18, Raasch teaches a computer program product comprising a computer*
14 *usable medium [138, FIG. 1] having computer readable program code means [BIOS:*
15 *col. 5, lines 18-21] embodied therein for causing data processing [col. 5, lines 18-31],*
16 *the computer readable program code means in said computer program product*
17 *comprising computer readable program code means [BIOS: col. 5, lines 18-21] for*
18 *causing a computer [100, FIG. 1] to effect the functions of the apparatus of claim 10 - as*
19 *the BIOS would cause the computer to effect the functions of any apparatus, hence*
20 *including the functions of the apparatus of claim 10.*

21   *11. As per claim 20, Raasch teaches a program storage device [138, FIG. 1] readable by*
22 *machine [100, FIG. 1], tangibly embodying a program of instructions [BIOS: col. 5,*
23 *lines 18-21] executable by the machine to perform method steps for transferring*
24 *interrupts [col. 4, lines 66-68], said method steps comprising the steps of claim 11 (the*
25 *BIOS would cause a computer to effect the steps of any method, hence including the steps*
26 *of the method of claim 11).*

27 In response, the applicants respectfully states that Raasch is not concerned with or teach.

28 indications of events or a preset condition as in the claims. The cited Raasch portion col. 5, lines

29 18-21 reads:

30   The keyboard interrupt service routine may be located in the RAM 120 or it may be

31   located in the ROM 138. Generally, the keyboard interrupt service routine for the

32   keyboard is provided as a basic operating function of the computer system 100 and is

33   stored in the ROM 138 as part of the Basic Input/Output System (BIOS) of the computer

34   system.

1   The cited Raasch portion col. 4, lines 66-68 reads:

2   The interrupt controller 130, the DMA controller 132 and the interface circuitry 134

3   provide communications between the processor bus 114 and an ISA bus 140.

4   This apparently fails to show the elements of claims 17-20. Thus, all claim 17-20 are allowable.

5   ***Response to Arguments***

6   *12.   Applicant's arguments with respect to the pending claims have been fully*
7   *considered but they are not persuasive or moot in view of the new grounds of rejections.*

8   *13.   Applicant's arguments with respect to the 112 rejections are moot in view of the*
9   *new ground of rejection.*

10   *14.   Applicant argues with respect to the art rejection that Raasch is not concerned*
11   *with indications of events or a preset condition. The argument is not persuasive because*
12   *Raasch was not relied upon to teach indications of events or a preset condition, because*
13   *the claims do not require such limitations, and because applicant appears to misinterpret*
14   *the rejections.*

15   *Claim 17 only requires a program code means for causing transfer of interrupts, and a*
16   *program code means for causing a computer to effect all functions of the apparatus of*
17   *claim 1. Claim 18 only requires a program code means for causing a computer to effect*
18   *all functions of the apparatus of claim 10. Claim 19 only requires a program code means*
19   *for causing transfer of interrupts, and a program code means for causing a computer to*
20   *effect all steps of the method of claim II. Claim 20 only requires a program of*
21   *instructions to perform method steps for transferring interrupts, the method steps*
22   *comprising steps of the method steps of the method of claim 11.*

23   *To the extent claimed, Raasch teaches a program code means causing transfer of*
24   *interrupts of claims 17, 19; a program code means for causing a computer to effect all*
25   *functions of claims 1, 10 (as claimed in claims 17-18); a program code means for*
26   *causing a computer to effect all steps of claim 11 (as claimed in claim 19); a program of*
27   *instructions to perform method steps for transferring interrupts of claim 20, the method*
28   *steps comprising all steps of the method of claim 11 - because Raasch teaches a BIOS*
29   *and a BIOS would cause a computer to effect the functions of any apparatus, and*
30   *because a BIOS would cause a computer to effect/perform the steps of any method.*

31   *Note that the claims do not recite any function/step that requires limitations concerned*
32   *with indications of events or preset condition.*

33   In response, the applicants respectfully states that indeed the cited art fails to anticipate the steps

34   of claims 17-20.

1   *15.   In addition, to help the examiner better understand the scope of the claimed*
2   *invention and further the prosecution, the examiner requests that applicant identify -*
3   *by reference to labels in the drawings, and/or page and line numbers in the*
4   *specification - the following elements and/or steps:*

5   *elements: apparatus, buffer, indications of interrupts, plurality of ports, peripheral*
6   *device, host computer system, controller (in claim 1); communications device (in*
7   *claims 8-9); data communications network interface (in claims 9-10); host processing*
8   *system, data processing system (in claim 10)*

9   *steps: the apparatus transferring interrupts, moving the contents of the buffer to the*
10   *payload portion of the control data block (claim 1); storing interrupts, moving the*
11   *contents of the buffer to the corresponding fields of the payload portion (in claim 11).*

12   *10. As per claim 18, Raasch teaches a computer program product comprising a computer*
13   *usable medium [138, FIG. 1] having computer readable program code means [BIOS:*
14   *col. 5, lines 18-21] embodied therein for causing data processing [col. 5, lines 18-31],*
15   *the computer readable program code means in said computer program product*
16   *comprising computer readable program code means [BIOS: col. 5, lines 18-21] for*
17   *causing a computer [100, FIG. 1] to effect the functions of the apparatus of claim 10 - as*
18   *the BIOS would cause the computer to effect the functions of any apparatus, hence*
19   *including the functions of the apparatus of claim 10.*

20   *11. As per claim 20, Raasch teaches a program storage device [138, FIG. 1] readable by*
21   *machine [100, FIG. 1], tangibly embodying a program of instructions [BIOS: col. 5,*
22   *lines 18-21] executable by the machine to perform method steps for transferring*
23   *interrupts [col. 4, lines 66-68], said method steps comprising the steps of claim 11 (the*
24   *BIOS would cause a computer to effect the steps of any method, hence including the steps*
25   *of the method of claim 11).*

26   In response, the applicants respectfully states that Raasch as stated above, Raasch is not

27   concerned with or teach. indications of events or a preset condition as in the claims. The cited

28   Raasch portion col. 5, lines 18-21 reads:

29   The keyboard interrupt service routine may be located in the RAM 120 or it may be

30   located in the ROM 138. Generally, the keyboard interrupt service routine for the

31   keyboard is provided as a basic operating function of the computer system 100 and is

32   stored in the ROM 138 as part of the Basic Input/Output System (BIOS) of the computer

33   system.

1   The cited Raasch portion col. 4, lines 66-68 reads:

2   The interrupt controller 130, the DMA controller 132 and the interface circuitry 134

3   provide communications between the processor bus 114 and an ISA bus 140.

4   This apparently fails to show the elements of claims 17-20. Thus, all claim 17-20 are allowable.

5   *Response to Arguments*

6   *12.   Applicant's arguments with respect to the pending claims have been fully*
7   *considered but they are not persuasive or moot in view of the new grounds of rejections.*

8   *13.   Applicant's arguments with respect to the 112 rejections are moot in view of the*
9   *new ground of rejection.*

10   *14.   Applicant argues with respect to the art rejection that Raasch is not concerned*
11 *with indications of events or a preset condition. The argument is not persuasive because*
12 *Raasch was not relied upon to teach indications of events or a preset condition, because*
13 *the claims do not require such limitations, and because applicant appears to misinterpret*
14 *the rejections.*

15 *Claim 17 only requires a program code means for causing transfer of interrupts, and a*
16 *program code means for causing a computer to _effect_ all functions of the apparatus of*
17 *claim 1. Claim 18 only requires a program code means for causing a computer to _effect_*
18 *all functions of the apparatus of claim 10. Claim 19 only requires a program code means*
19 *for causing transfer of interrupts, and a program code means for causing a computer to*
20 *_effect_ all steps of the method of claim 11. Claim 20 only requires a program of*
21 *instructions to _perform method steps for transferring interrupts_, the method steps*
22 *comprising steps of the method steps of the method of claim 11.*

23 *To the extent claimed, Raasch teaches a program code means causing transfer of*
24 *interrupts of claims 17, 19; a program codemeans for causing a computer to _effect_ all*
25 *functions of claims 1, 10 (as claimed in claims 17-18); a program code means for*
26 *causing a computer to _effect_ all steps of claim 11 (as claimed in claim 19); a program of*
27 *instructions to perform method steps for transferring interrupts of claim 20, the method*
28 *steps comprising all steps of the method of claim 11 - because Raasch teaches a BIOS*
29 *and a BIOS would cause a computer to effect the functions of any apparatus, and*
30 *because a BIOS would cause a computer to effect/perform the steps of any method.*

31 *Note that the claims do not recite any function/step that requires limitations concerned*
32 *with indicationsof events or preset condition.*

33   *15.   In addition, to help the examiner better understand the scope of the claimed*
34 *invention and further the prosecution, the examiner requests that applicant identify -*

1 *by reference to labels in the drawings, and/or page and line numbers in the*
2 *specification - the following elements and/or steps:*

3 *elements: apparatus, buffer, indications of interrupts, plurality of ports, peripheral*
4 *device, host computer system, controller (in claim 1); communications device (in*
5 *claims 8-9); data communications network interface (in claims 9-10); host processing*
6 *system, data processing system (in claim 10)*

7 *steps: the apparatus transferring interrupts, moving the contents of the buffer to the*
8 *payload portion of the control data block (claim 1); storing interrupts, moving the*
9 *contents of the buffer to the corresponding fields of the payload portion (in claim 11).*

10 In response, the applicants respectfully states that applicants hold the correctness of the

11 previously stated remarks.

12 Please charge any fee necessary to enter this paper to deposit account 50-0510.

13   Respectfully submitted,

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